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Shams, M.; Ebergen, J.C.; Elmasry, M.I.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 6 , Issue: 4 , Dec. 1998
Pages:563 - 567

[\[Abstract\]](#) [\[PDF Full-Text \(84KB\)\]](#) **IEEE JNL****2 On the delay-sensitivity of gate networks**

Brzozowski, J.A.; Ebergen, J.C.;
Computers, IEEE Transactions on , Volume: 41 , Issue: 11 , Nov. 1992
Pages:1349 - 1360

[\[Abstract\]](#) [\[PDF Full-Text \(1000KB\)\]](#) **IEEE JNL****3 DUDS: a fault abstraction and collapsing framework for asynchronous circuits**

Shirvani, P.P.; Mitra, S.; Ebergen, J.C.; Roncken, M.;
Advanced Research in Asynchronous Circuits and Systems, 2000. (ASYNC 2000) Proceedings. Sixth International Symposium on , 2-6 April 2000
Pages:73 - 82

[\[Abstract\]](#) [\[PDF Full-Text \(184KB\)\]](#) **IEEE CNF****4 Optimizing CMOS Implementations of the C-element**

Shams, M.; Ebergen, J.C.; Elmasry, M.I.;
Computer Design: LSI in Computers and Processors, 1997. ICCD '97. Proceedings., 1997 IEEE International Conference on , 12-15 Oct. 1997
Pages:700 - 705

[\[Abstract\]](#) [\[PDF Full-Text \(1180KB\)\]](#) **IEEE CNF****5 A comparison of CMOS implementations of an asynchronous circuits primitive: the C-element**

Shams, M.; Ebergen, J.C.; Elmasry, M.I.;
Low Power Electronics and Design, 1996., International Symposium on , 12-14 Aug. 1996
Pages:93 - 96

[\[Abstract\]](#) [\[PDF Full-Text \(336KB\)\]](#) **IEEE CNF****6 Predicting performance of micropipelines using Charlie diagrams**

Ebergen, J.C.; Fairbanks, S.; Sutherland, I.E.;
Advanced Research in Asynchronous Circuits and Systems, 1998. Proceedings. 1998 Fourth International Symposium on , 30 March-2 April 1998
Pages:238 - 246

[\[Abstract\]](#) [\[PDF Full-Text \(116KB\)\]](#) **IEEE CNF**

7 Delay-insensitive solutions to the committee problem

Benko, I.; Ebergen, J.C.;

Advanced Research in Asynchronous Circuits and Systems, 1994.,
Proceedings of the International Symposium on , 3-5 Nov. 1994

Pages:228 - 237

[\[Abstract\]](#) [\[PDF Full-Text \(756KB\)\]](#) **IEEE CNF**

8 A verifier for network decompositions of command-based specifications

Ebergen, J.C.; Gingras, S.;

System Sciences, 1993, Proceeding of the Twenty-Sixth Hawaii International
Conference on , Volume: i , 5-8 Jan 1993

Pages:310 - 318 vol.1

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suitable for cryptographic hardware

Tenca, A.F.; Tawalbeh, L.A.;

Electronics Letters, Volume: 40, Issue: 5, 4 March 2004

Pages:304 - 306

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2 A VLSI algorithm for modular multiplication/division

Kaihara, M.E.; Takagi, N.;

Computer Arithmetic, 2003. Proceedings. 16th IEEE Symposium on, 15-18

June 2003

Pages:220 - 227

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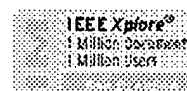
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(galois) <and> counter <and> division

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1 New systolic architectures for inversion and division in GF(2/sup m/)

Yan, Z.; Sarwate, D.V.;

Computers, IEEE Transactions on , Volume: 52 , Issue: 11 , Nov. 2003

Pages:1514 - 1519

[\[Abstract\]](#) [\[PDF Full-Text \(585 KB\)\]](#) **IEEE JNL**

2 High-speed easily testable Galois-field Inverter

Chih-Tsun Huang; Cheng-Wen Wu;

Circuits and Systems II: Analog and Digital Signal Processing, IEEE

Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Volume: 47 , Issue: 9 , Sept. 2000

Pages:909 - 918

[\[Abstract\]](#) [\[PDF Full-Text \(324 KB\)\]](#) **IEEE JNL**

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Tenca, A.F.; Tawalbeh, L.A.;

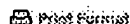
Electronics Letters , Volume: 40 , Issue: 5 , 4 March 2004

Pages:304 - 306

[\[Abstract\]](#) [\[PDF Full-Text \(192 KB\)\]](#) **IEE JNL**
2 A VLSI algorithm for modular multiplication/division
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